

Applicants: Sarah E. Kim et al.

THICK METAL LAYER INTEGRATED PROCESS FLOW TO  
IMPROVE POWER DELIVERY AND MECHANICAL  
BUFFERING

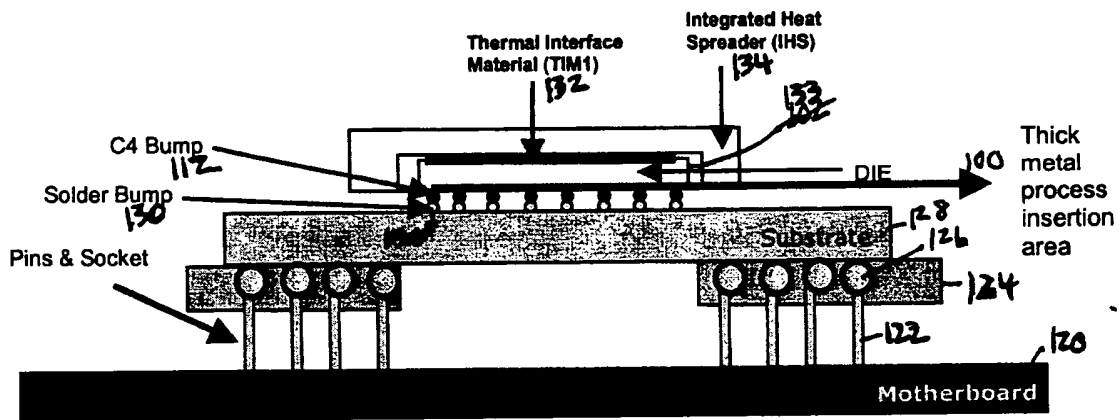
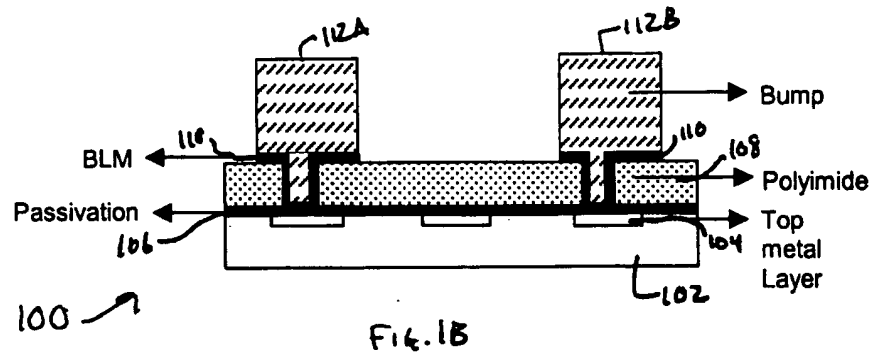


FIG. 1A

↑ 150

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FIG. 1C

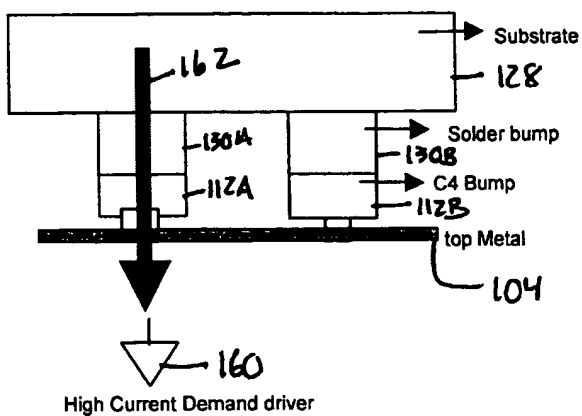
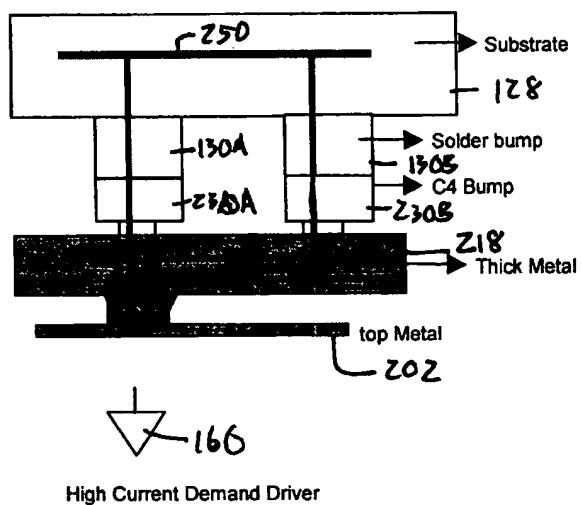


FIG. 1D



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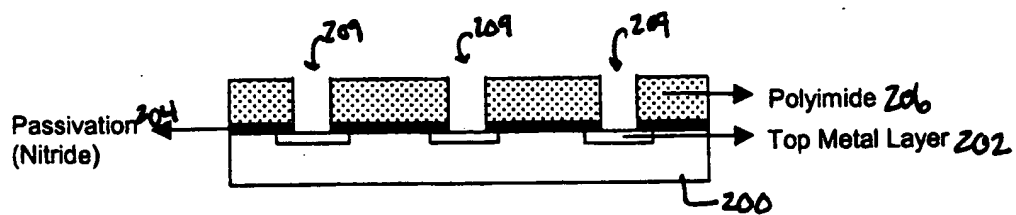


FIG. 2

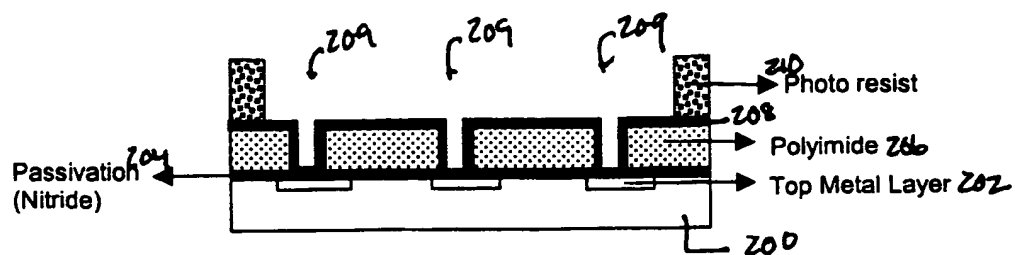


FIG. 3

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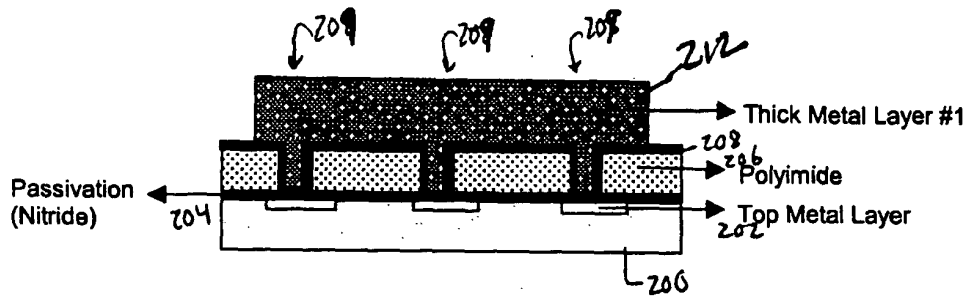
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FIG. 4

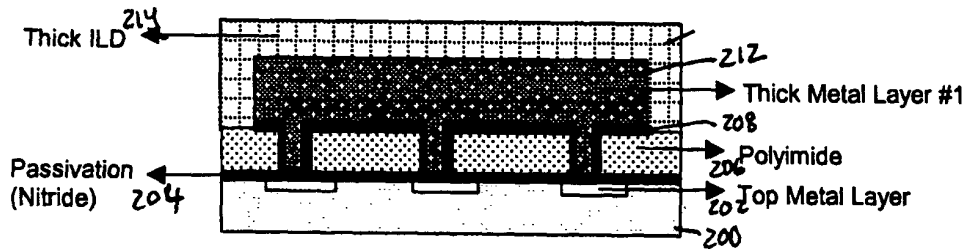


FIG. 5

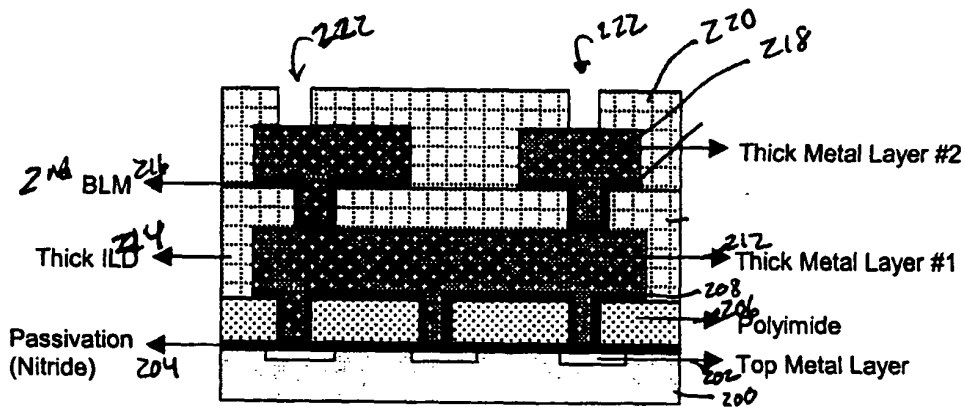
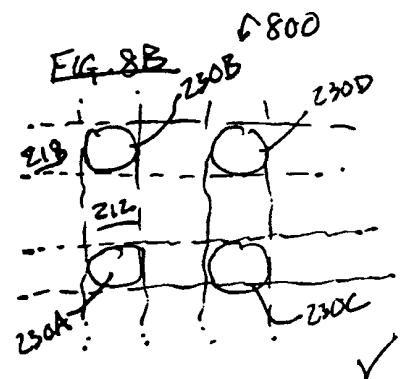
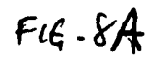
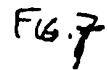


FIG. 6

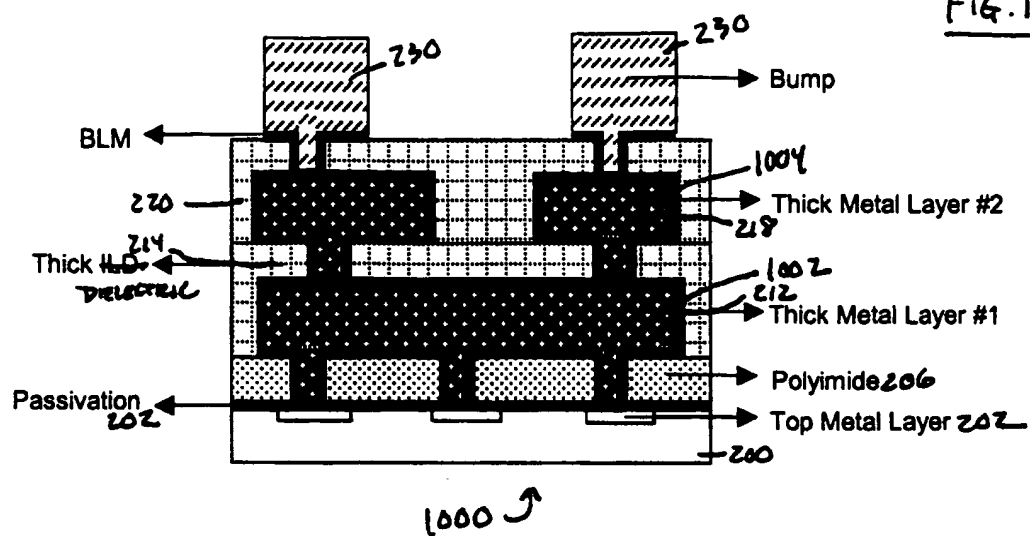


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Fig. 9A Flow 1	Fig. 9B Flow 2	Fig. 11A Flow 3	Fig. 11B Flow 4
1. No Cu diffusion Barrier Needed	1. No Cu diffusion Barrier Needed	1. Need Cu diffusion Barrier	1. Need Cu diffusion Barrier
2. Use photo-definable ILD	2. Use self-planarizing ILD	2. Use photo-definable ILD	2. Use self-planarizing ILD
Passivation Dep (Nitride) 900	Passivation Dep (Nitride) 900	Passivation Dep (Nitride) 900	Passivation Dep (Nitride) 900
Polyimide Pattern 902	Polyimide Pattern 902	Polyimide Pattern 902	Polyimide Pattern 902
Develop Polyimide 904	Develop Polyimide 904	Develop Polyimide 904	Develop Polyimide 904
BLM Dep 906	BLM Dep 906	BLM Dep 906	BLM Dep 906
PR Coating 908	PR Coating 908	PR Coating 908	PR Coating 908
PR (Thick Metal Layer #1) Pattern 910	PR (Thick Metal Layer #1) Pattern 910	PR (Thick Metal Layer #1) Pattern 910	PR (Thick Metal Layer #1) Pattern 910
Cu Plating 912	Cu Plating 912	Cu Plating 912	Cu Plating 912
Resist Strip 914	Resist Strip 914	Resist Strip 914	Resist Strip 914
BLM Etch/Ash 916	BLM Etch/Ash 916	BLM Etch/Ash 916	BLM Etch/Ash 916
Deposit dielectric 918A (photo-definable polymer)	Deposit dielectric 918B (self-planarizing polymer)	EL diffusion barrier plating 1100	EL diffusion barrier plating 1100
Photo-pattern vias 920	PR Coating 924	Deposit dielectric 918A (photo-definable polymer)	Deposit dielectric 918B (self-planarizing polymer)
Develop dielectric 922	Pattern vias 926	Photo-pattern vias 920	PR Coating 924
BLM Dep 924	Etch dielectric (Dry) 928	Develop dielectric 922	Pattern vias 926
PR Coating 926	PR Strip 930	BLM Dep 924	Etch dielectric (Dry) 928
PR (Thick Metal Layer #2) Pattern 928	BLM Dep 924	PR Coating 926	PR Strip 930
Cu Plating 930	PR Coating 926	PR (Thick Metal Layer #2) Pattern 928	BLM Dep 924
Resist Strip 932	PR (Thick Metal Layer #2) Pattern 928	Cu Plating 930	PR Coating 926
BLM Etch/Ash 934	Cu Plating 930	Resist Strip 932	PR (Thick Metal Layer #2) Pattern 928
Deposit dielectric 936 (photo-definable polymer)	Resist Strip 932	BLM Etch/Ash 934	Cu Plating 930
Photo-pattern vias 938	BLM Etch/Ash 934	EL diffusion barrier plating 1102	Resist Strip 932
Develop dielectric 940	Deposit dielectric 936 (self-planarizing polymer)	Deposit dielectric 936 (photo-definable polymer)	BLM Etch/Ash 934
BLM Dep 942	PR Coating 936	Photo-pattern vias 938	EL diffusion barrier plating 1102
PR Coating 944	Pattern vias 936	Develop dielectric 940	Deposit dielectric 936 (self-planarizing polymer)
Bump Pattern 946	Etch dielectric (Dry) 938	BLM Dep 942	PR Coating 936
Bump Plating 948	PR Strip 940	PR Coating 944	Pattern vias 936
Resist Strip 950	BLM Dep 942	Bump Pattern 946	Etch dielectric (Dry) 938
BLM Etch/Ash 952	PR Coating 944	Bump Plating 948	PR Strip 940
	Bump Pattern 946	Resist Strip 950	BLM Dep 942
	Bump Plating 948	BLM Etch/Ash 952	PR Coating 944
	Resist Strip 950		Bump Pattern 946
	BLM Etch/Ash 952		Bump Plating 948
			Resist Strip 950
			BLM Etch/Ash 952

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Fig.

Flow 5	
Use Cu CMP process	
1st	Passivation Dep (Nitride) 1200
	Deposit dielectric 1200
	PR Coating 1202
	Pattern vias 1204
	PR Coating 1206
	PR (Thick Metal Layer #1) Pattern 1208
	BLM Dep 1210
	Cu plating 1212
	Cu CMP 1214
	Passivation Dep (Nitride) 1216
2nd	Deposit dielectric 1218
	PR Coating 1220
	Pattern vias 1222
	PR Coating 1224
	PR (Thick Metal Layer #2) Pattern 1226
	BLM Dep 1228
	Cu plating 1230
	Cu CMP 1232
	Passivation Dep (Nitride) 1234
	Polyimide Pattern Develop polyimide 1236
3rd	BLM Dep 1238
	PR Coating 1240
	Bump Pattern 1242
	Bump Plating 1244
	Resist Strip 1246
	BLM Etch/Ash 1248

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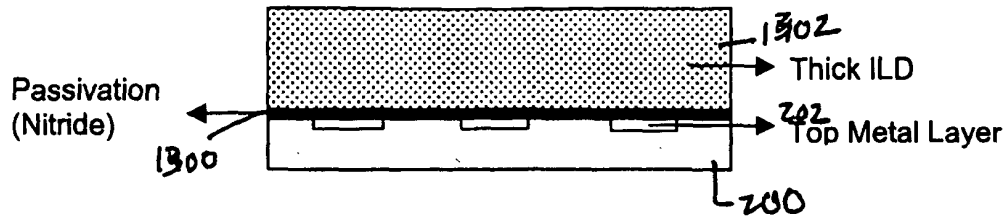
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FIG. 13A

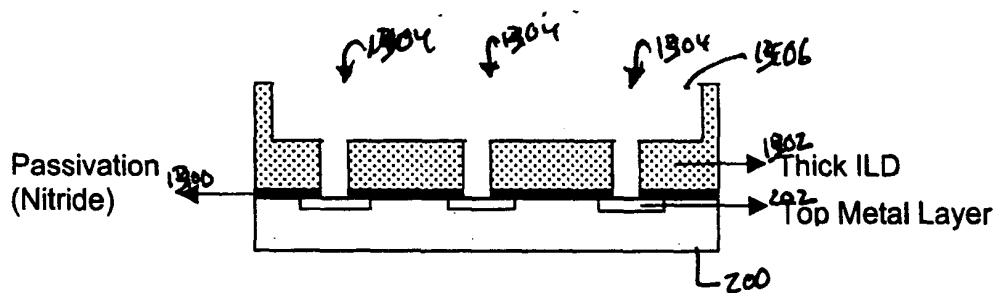


FIG. 13B

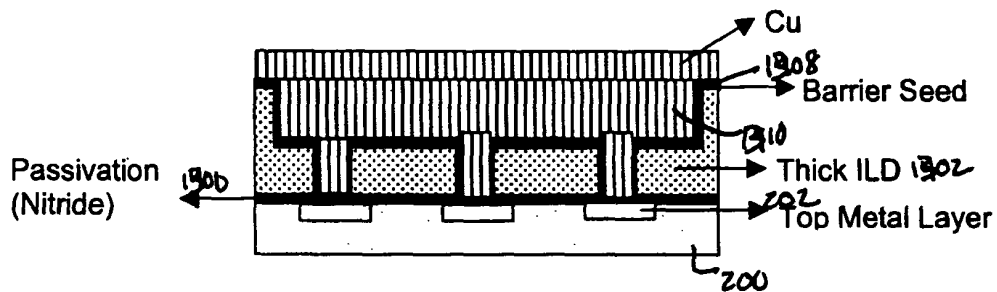


FIG. 13C

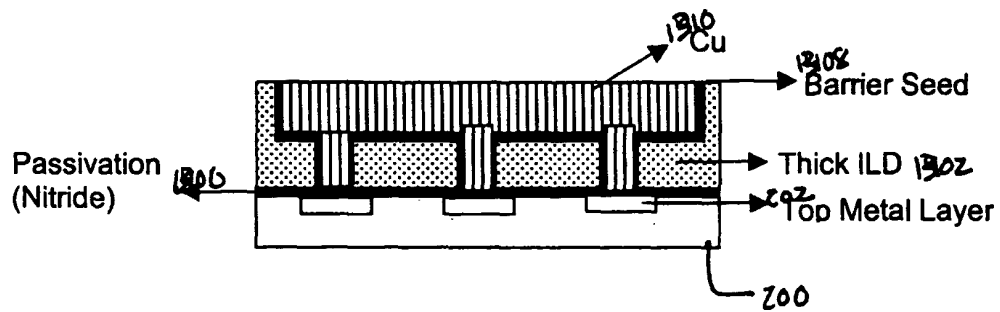
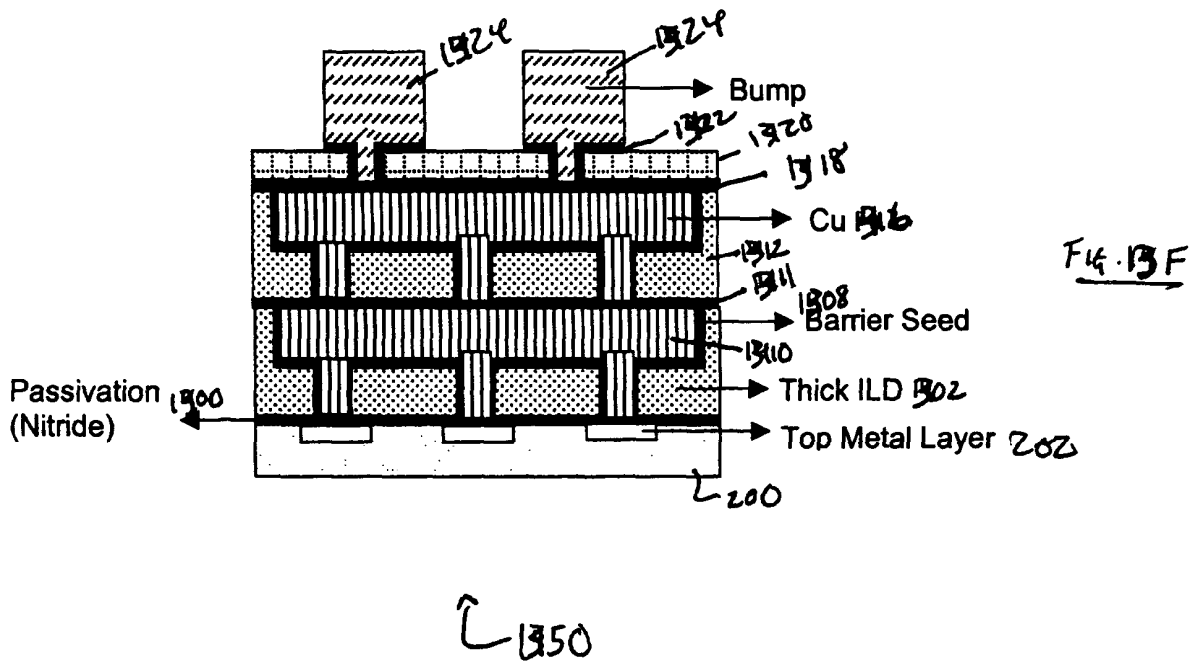
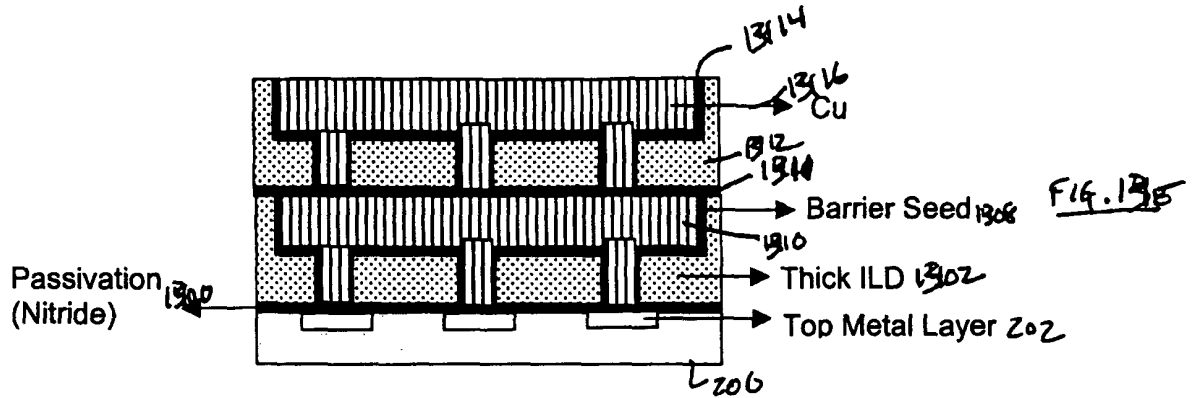


FIG. 13D

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Simulation Parameters			Results	
Additional Thick Metal Layers	Metal Width	Via Resistance (m $\Omega$ )	I <sub>max</sub> (mA)	IR Drop (mV)
1410 - Default (present state of art)			680	29
1400 - Two 45 $\mu$ m thick metal layers	70 $\mu$ m for Metal layer #2 100 $\mu$ m for Metal layer #1	0.7	430 (36% I <sub>max</sub> improvement)	30
1402 - Two 15 $\mu$ m thick metal layers	70 $\mu$ m for Metal layer #2 100 $\mu$ m for Metal layer #1	0.7	530 (22% I <sub>max</sub> improvement)	30
1404 - Two 45 $\mu$ m thick metal layers	70 $\mu$ m for Metal layer #2 100 $\mu$ m for Metal layer #1	70	370 (46% I <sub>max</sub> improvement)	49
1406 - Two 15 $\mu$ m thick metal layers	70 $\mu$ m for Metal layer #2 100 $\mu$ m for Metal layer #1	70	380 (44% I <sub>max</sub> improvement)	51

FIG. 14

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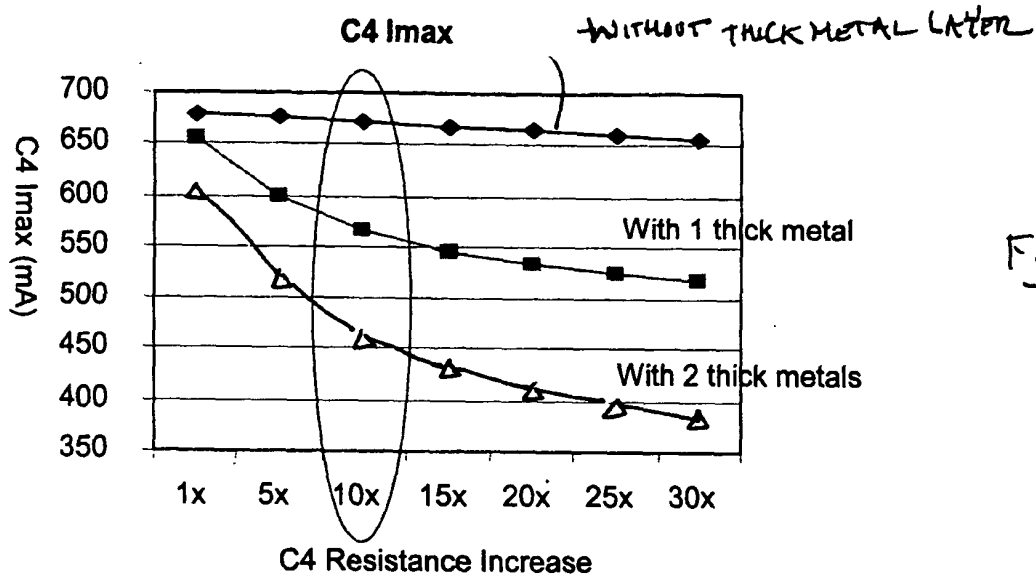


FIG. 15A

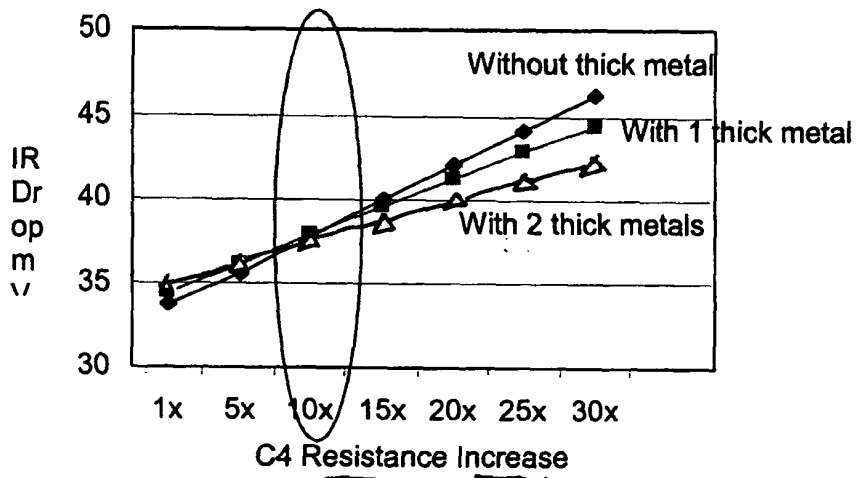
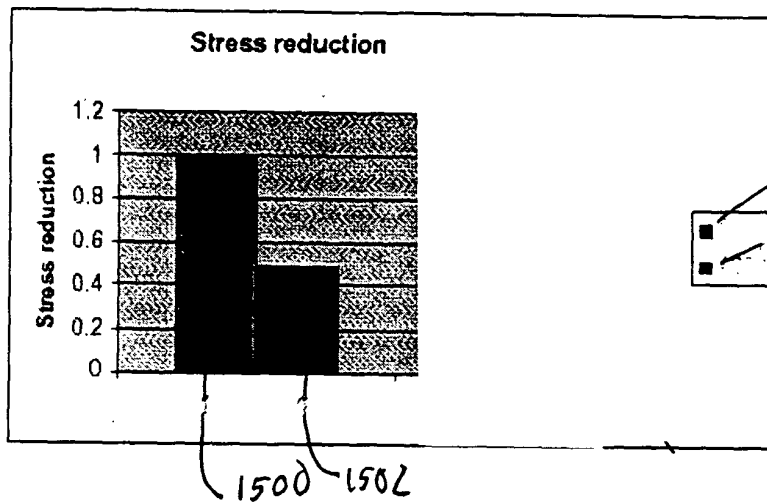


FIG. 15B

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WITHOUT THICK METAL LAYERS  
WITH THICK METAL LAYERS  
FIG 16